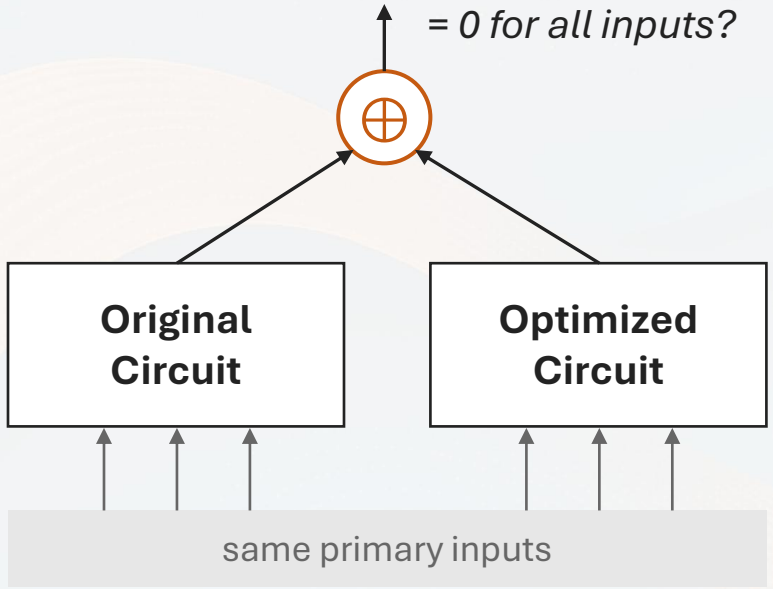


Heterogeneous Synergy:
Fusing SAT Solvers and GPU Simulation for CEC

Yang Sun[1], **Tianji Liu**[2], Martin D.F. Wong[3], Evangeline F.Y. Young[1]

[1]The Chinese University of Hong Kong [2]Institute of Computing Technology, CAS [3]Hong Kong Baptist University

Combinational Equivalence Checking (CEC)

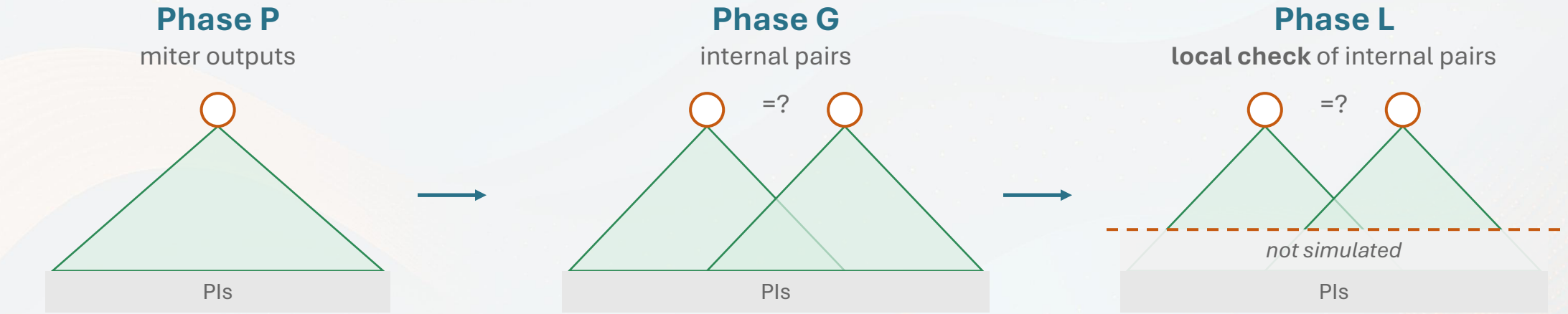


miter: equivalent ⇔
every output is constant 0

- **SAT sweeping** (e.g., ABC &cec), repeated until done:
  - 1. **simulate** random patterns → candidate pairs
  - 2. **prove** each pair using SAT solver
  - 3. **merge** proven pairs → miter size reduced
- Simulation only *guesses*; **SAT does all the proving**
- CEC is co-NP-complete, so it does not scale easily: **voter_10xd** (22M-node miter) takes **15.1 h** in ABC

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DAC'25: Proving by Exhaustive Simulation



all $2^{|supp|}$ patterns of the PO's support

patterns of the union of the pair's supports

all $2^{|C|}$ patterns of a common cut C

Limitations

- A local check can **prove** equality but **never disprove** it: a mismatch may be an unreachable pattern at the cut leaves (satisfiability don't care, SDC)
- No compact common cut ⇒ no trial at all. Leftover pairs go to **ABC &cec** at the end
- **sqrt_10xd**: GPU 36 s, then the ABC fallback **19,810 s** (99.8% of the runtime)

Tianji Liu, Evangeline F.Y. Young, "Simulation-based Parallel Sweeping: A New Perspective on Combinational Equivalence Checking," Proc. DAC, 2025.

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Simulation and SAT: Pros and Cons

GPU simulation (local check)

+ Regular, data-parallel: one sweep checks **thousands** of pairs
+ Cheap per pair
− Needs a compact common cut
− Can only prove, not disprove

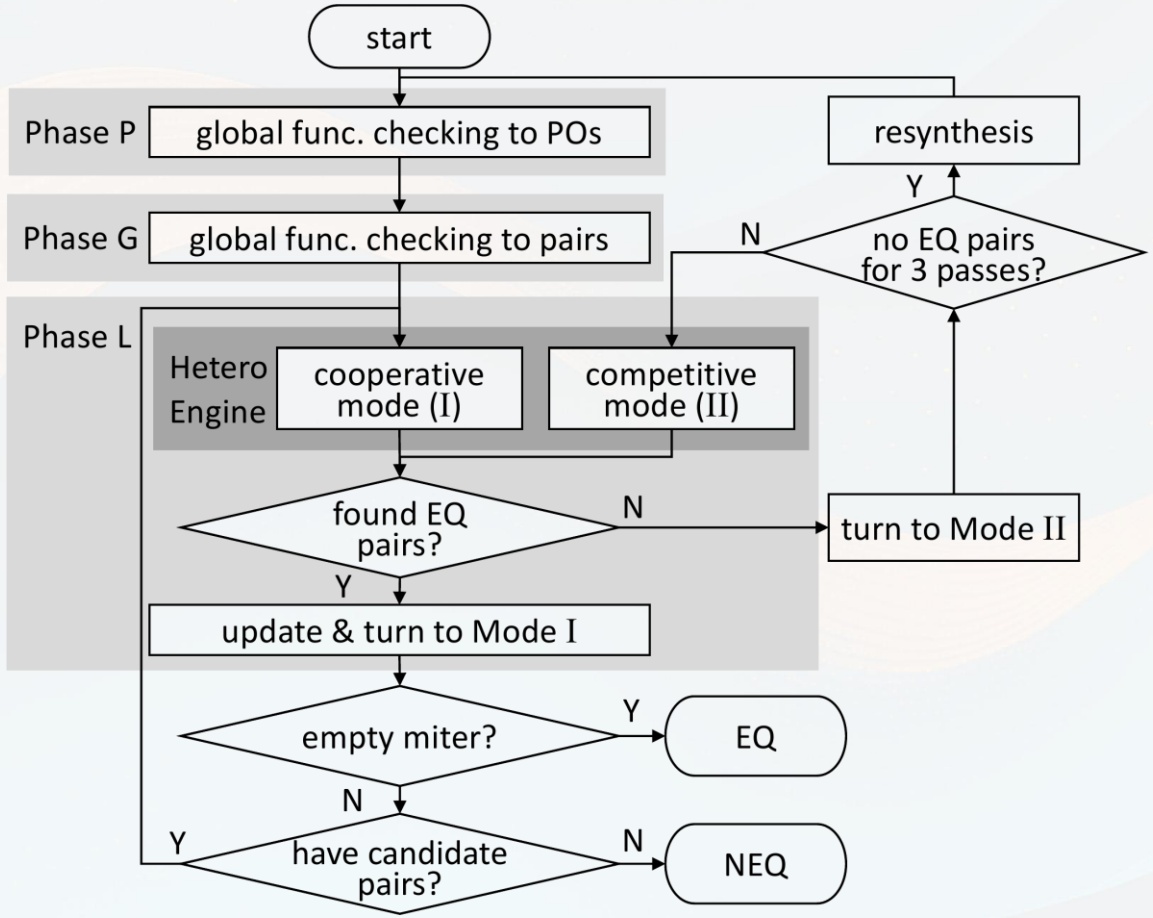
CPU SAT solving (global check)

− Irregular, branchy search: suits a **CPU**, not a GPU
− Much more expensive per pair
+ Does not need a compact cut
+ Can **prove (EQ) and disprove (NEQ)**

Our solution: **use both in one framework, each on its own processor, to combine their strengths**

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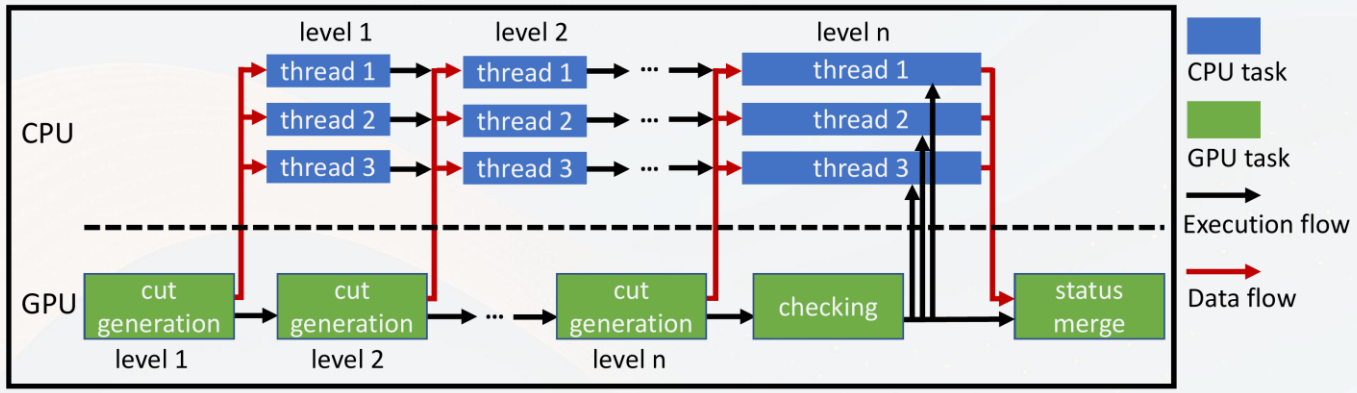
Heterogeneous CEC Framework



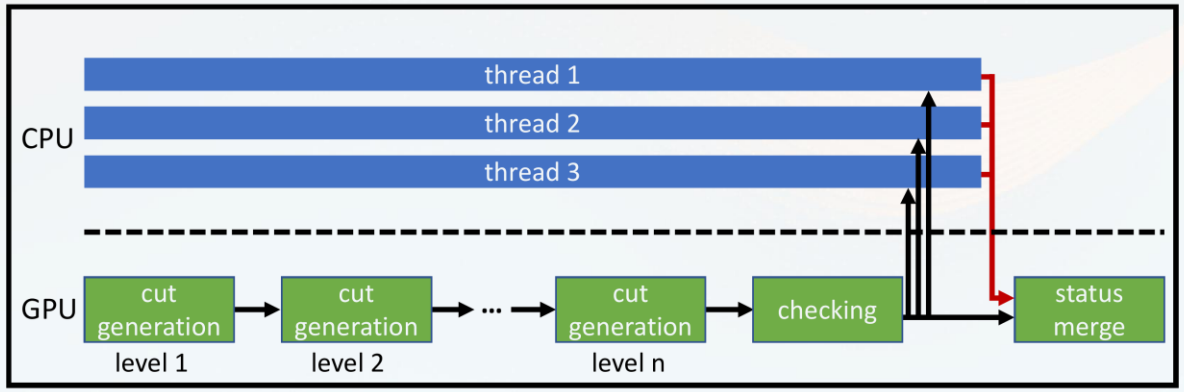
- **P** and **G** as in DAC'25; **L** is the loop we change
- Each pass: GPU simulation + CPU SAT on one miter; proofs from either side shrink it
- Three techniques:
  - scheduling in two modes
  - iterative sieving (adjusting SAT effort)
  - adaptive resynthesis (restructuring)
- **No external checker required**

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Scheduling in Two Modes



(a) Flow of cooperative mode



(b) Flow of competitive mode

Cooperative (default)

- GPU: level-wise cut generation
- Pairs without a valid cut go to **CPU SAT** at once, pipelined

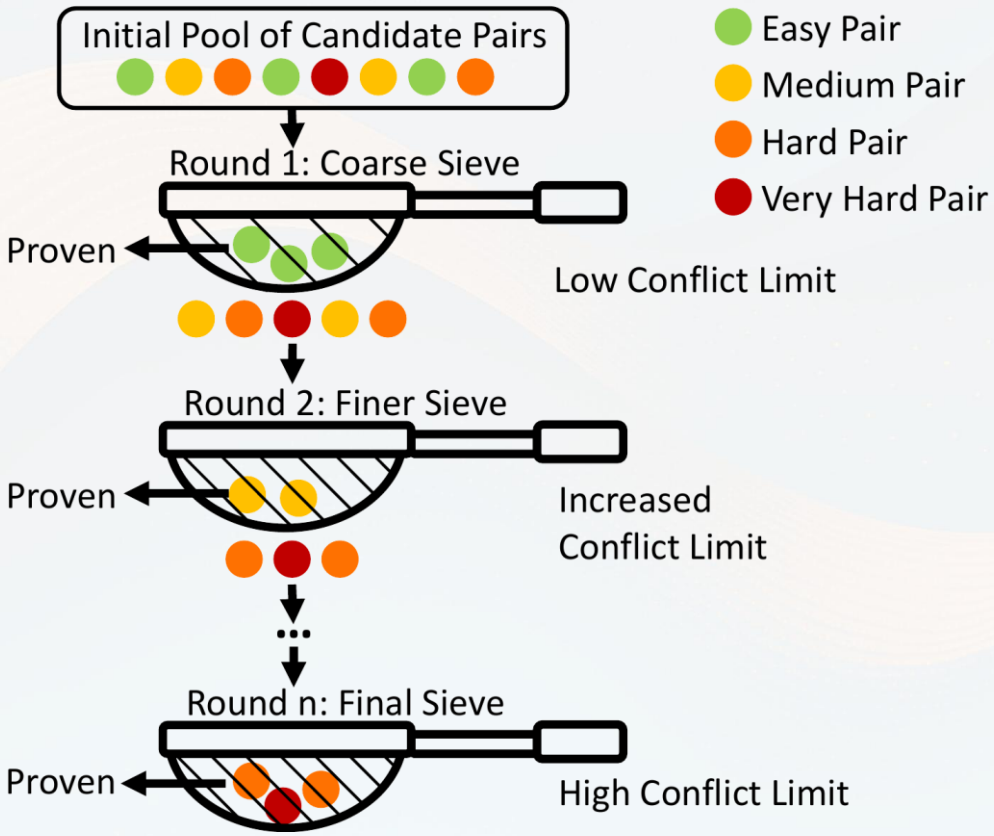
Competitive (after a stall)

- All pairs to SAT from the beginning; GPU races on the same pairs
- EQ from either side, NEQ only from SAT

Mode Switch: proven EQ → cooperative; EQ not found → competitive

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Breaking Verification Stalls



Iterative sieving (SAT effort)

- **Conflict limit** per pair: starts low, doubles when undetermined > resolved
- **Processed-pair quota**: keeps SAT busy after the GPU finishes; doubles when the GPU proves nothing

⇒ easy pairs first, hard pairs later

Adaptive resynthesis (restructure)

- After **3 passes** with no new EQ, restructure the whole miter (GPU resubstitution [1])
- New structure ⇒ new opportunities (cuts, SAT instances)

[1] Yang Sun, Tianji Liu, Martin D.F. Wong, Evangeline F.Y. Young, "Massively Parallel AIG Resubstitution," Proc. DAC, 2024.

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Soundness and Completeness

Sound (proven miter is EQ)

- GPU proof is done by exhaustive simulation
- A mismatch in GPU local check may be an SDC, so NEQ always comes from SAT
- **Every miter update, including resynthesis, preserves its function**

Complete (EQ miter can be proven)

- Node count is finite and never increases
- Conflict limit and quota keep growing on stalls

⇒ **every pair can be decided after finitely many passes**

NEQ check: all 11 non-equivalent ICCAD 2015 EC/ECO contest cases reported NEQ

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Results

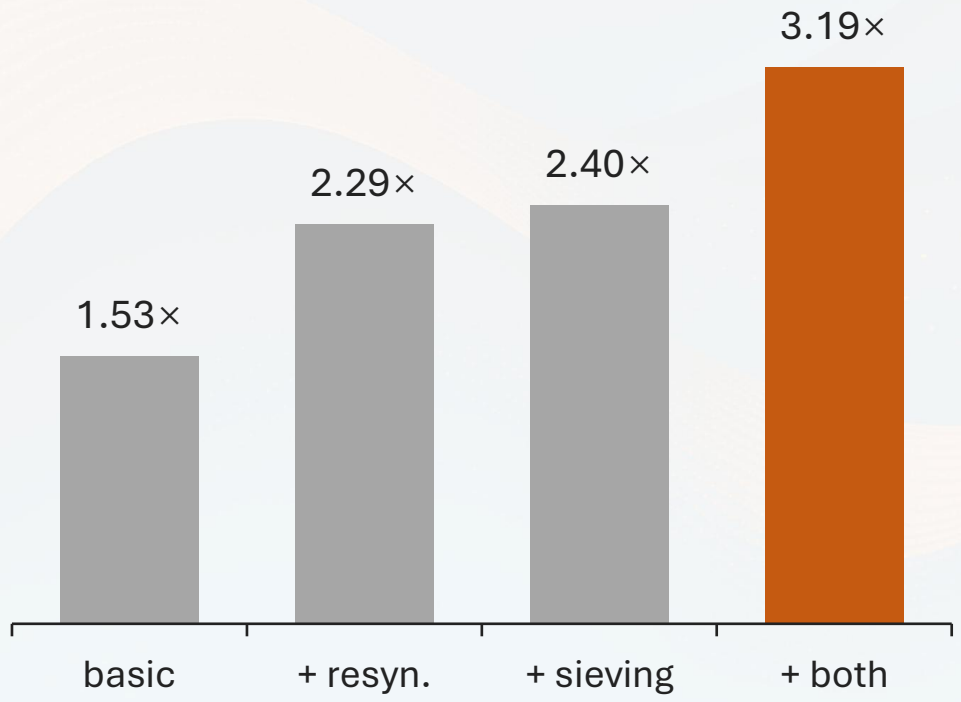
Platform: Xeon 8369B + one A100 GPU · Ours: 16 SAT solvers (same SAT solver as ABC &cec) · Conformal (Cfm): 16 CPU threads
Benchmarks: EPFL + IWLS, up to 52.6M miter nodes, original vs. resyn2

Runtime (s)	ABC &cec	Conformal	DAC'25	Ours	vs. ABC	vs. Cfm	vs. DAC'25
hyp_7xd	8066	336982	3064	2574	3.13×	130.94×	1.19×
multiplier_10xd	2680	2795	85	86	31.34×	32.68×	0.99×
sqrt_10xd	21534	24790	19846	**1515**	14.21×	16.36×	**13.10×**
square_10xd	1096	2331	40	42	26.26×	55.82×	0.95×
voter_10xd	54422	1793	23981	**288**	**188.86×**	6.22×	**83.22×**
ac97_ctrl_10xd	250	1258	26	26	9.67×	48.61×	1.01×
vga_lcd_5xd	111	707	43	7	15.51×	98.61×	5.97×
leon2	21.8	1107	16.5	6.7	3.24×	164.49×	2.45×
leon3	27.1	651	22.0	6.6	4.09×	98.04×	3.31×
netcard	34.8	202	11.2	6.1	5.72×	33.22×	1.84×
Geomean					**12.29×**	**47.81×**	**3.19×**

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Analysis on Sieving and Resynthesis

Geomean speedup vs. DAC'25



Runtime (s)	basic	+ rs	+ sv	+ both
sqrt_10xd	4068	**1029**	4199	1515
vga_lcd_5xd	30.0	28.7	**8.9**	**7.2**
voter_10xd	45222	2017	2275	**288**

- **sqrt**: sieving alone does not help
- **vga_lcd**: resynthesis alone does not help
- **voter**: huge speedup with both techniques

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Summary

- A heterogeneous CEC engine: **GPU simulation** and **CPU SAT** work on one miter in a closed loop
- Three techniques for breaking stalls:
  cooperative / competitive scheduling, iterative sieving, adaptive resynthesis
- Sound and complete
- **12.29×** vs. ABC, **47.81×** vs. Conformal, **3.19×** vs. DAC'25

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Thank You!

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